Abstract

IDEC Chip Design Contest

Pseudo-Static n-type Gain Cell eDRAM Based Processing-In-Memory With 8-b MAC Operation

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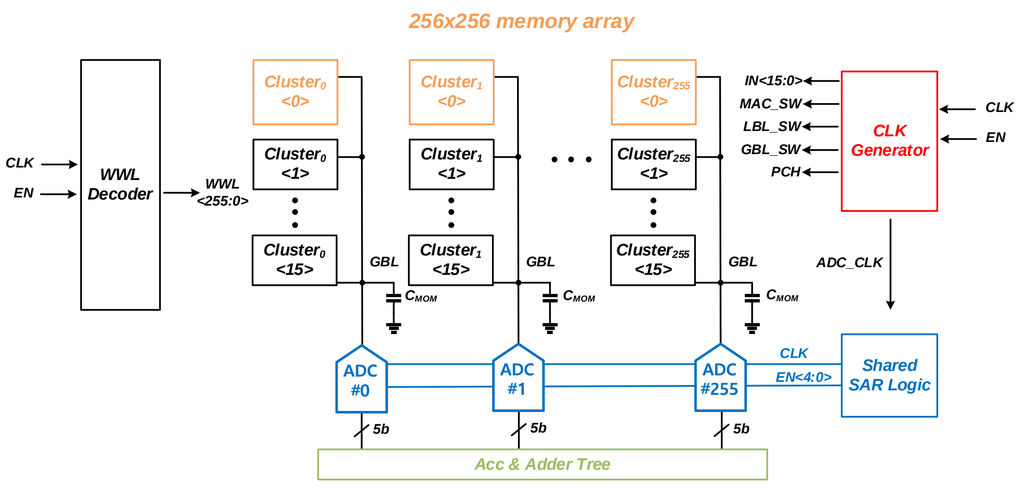
Abstract

This article presents a pseudo-static n-type gain cell (PS-nGC) embedded DRAM (eDRAM) based processing-in-memory (PIM). The proposed PIM based on the PS-nGC eDRAM has an advantage over SRAM based PIM in terms of area because it has one less transistor. Also, for efficient 8bit signed integer MAC operation, the accumulation is performed by Charge-Injection SAR ADC (CI SAR ADC) and bitwise accumulator.

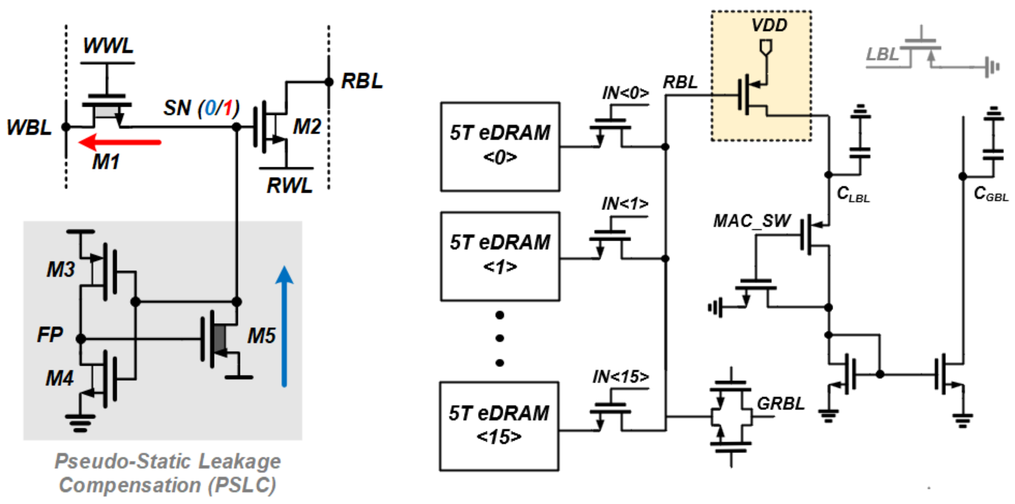
Proposed Design

- **Proposed PIM with PS-nGC eDRAM macro** consists of 256 x 256 cells, timing controller, CI SAR ADC and accumulator.
- **The PS-nGC 5T and current mirror** are consists of one cluster for multiply operation. Column of the proposed PIM macro is divided into 16 clusters.
- **CI SAR ADC and bitwise accumulator** accumulate the multiplied results.



Current Domain MAC Operation

- **The PS-nGC eDRAM consists of 5 transistors.** It can address the leakage issues in the conventional 2T1C gain cell.
- **Multiply operation** is performed with PS-nSC 5T and current mirror. As weight data is stored in PS-nGC 5T and input data is applied to the input transistor, AND operation is performed. The result is stored in Local Bit Line (LBL).
- **Current mirror** in each cluster transfers the results stored in LBL to Global Bit Line (GBL), and the light MAC operation in the current domain proceeds. The light MAC operation through the current mirror improves the linearity.



Hybrid Accumulation Operation

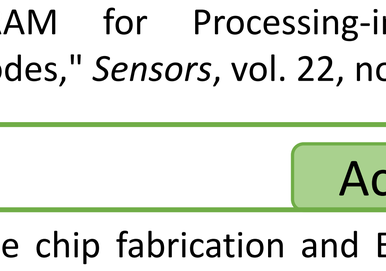
- **CI SAR ADC** converts the MAC operation value calculated through the cluster into a digital value. It is area-efficient because it uses a charge-injection cell based on long channel transistor instead of Capacitive DAC (CDAC).
- **Bitwise accumulator** is consists of full adder and shift register. It accumulates the digital value converted by the charge-injection SAR ADC. It consists of one per 8 column of PIM macro, and 8 bit signed MAC operation can be performed by changing the mode when calculating MSB of input or weight data.
- **Hybrid accumulation** is performed in the analog domain for energy efficiency at first stage and in the digital domain for high accuracy at second stage.

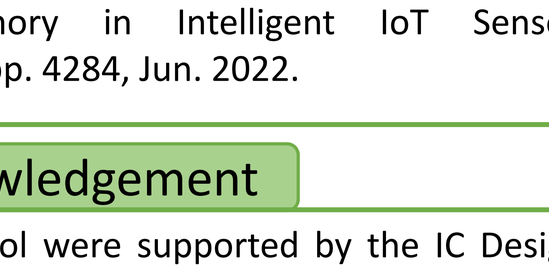
Input : signed int8
Weight : signed int8

CI SAR ADC RESULTS								sign extension
# shift	0	1	2	3	4	5	6	7
MAC value	Σ In[0]xW[0]	Σ In[0]xW[1]	Σ In[0]xW[2]	Σ In[0]xW[3]	Σ In[0]xW[4]	Σ In[0]xW[5]	Σ In[0]xW[6]	Σ In[0]xW[7]
MAC value bit	5bit	5bit	5bit	5bit	5bit	5bit	5bit	5bit
shift	5bit	6bit	5bit	6bit	5bit	6bit	5bit	7bit
add	8bit		8bit		8bit		8bit(substract)	
shift	8bit		10bit		8bit		10bit	
add	10bit				10bit			
shift	10bit				16bit			
add	16bit							

Simulations

- At the operating frequency of 200MHz, V_{GBL}, the light MAC operation result in current domain, is linear with the calculation result.
- The result of the MAC operation successfully performed through the current mirror is converted into the digital value through the CI SAR ADC.





Conclusions

This article presented an area-efficient PS-nGC based PIM to solve the retention time of the conventional eDRAM. The current mirror in the cluster multiplies the weight data stored in the PS-nGC 5T and the applied input data. The hybrid accumulation performed by CI SAR ADC and the bitwise accumulator can efficiently and accurately perform high bit accumulation.

Reference

Subin Kim and Jun-Eun Park, "Pseudo-Static Gain Cell of Embedded DRAM for Processing-in-Memory in Intelligent IoT Sensor Nodes," *Sensors*, vol. 22, no. 11, pp. 4284, Jun. 2022.

Acknowledgement

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